UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/051,916	01/17/2002	Ki-Hwan Song	5649-947	1803

20792 7590 10/22/2003

MYERS BIGEL SIBLEY & SAJOVEC
PO BOX 37428
RALEIGH, NC 27627

EXAMINER	
SHINGLETON, MICHAEL B	
ART UNIT	PAPER NUMBER
2817	

DATE MAILED: 10/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
10-051,916	Song et al.
Examiner	**Group Art Unit**
SHINGLETON	2817

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE Three MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

☒ Responsive to communication(s) filed on 8-11-2003.

☒ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

☒ Claim(s) 1-16, 18-25, 27-32 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☒ Claim(s) 16, 18-25, 27-32 is/are allowed.

☒ Claim(s) 1-3, 12, 13, 15 is/are rejected.

☒ Claim(s) 4-11, 14 is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement

Application Papers

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119 (a)-(d).

☐ All ☐ Some* ☐ None of the:

☐ Certified copies of the priority documents have been received.

☐ Certified copies of the priority documents have been received in Application No. _____.

☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a))

*Certified copies not received: _____.

Attachment(s)

☐ Information Disclosure Statement(s), PTO-1449, Paper No(s). _____

☐ Interview Summary, PTO-413

☐ Notice of Reference(s) Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. 6,483,764 (Hsu) in view of Vergis 6,453,218 (Vergis).

Columns 1 and 2 of Hsu describe an integrated circuit memory device, i.e. DRAM chip (See in particular column 1, lines 57-67 and column 2, lines 1-17). This device includes a clock generation circuit that takes the form of a refresh circuit. Hsu specifically recites that the refresh circuit has a control circuit that receives the signal from a temperature sensor (See column 1, around line 59). This control circuit generates a refresh signal according to a ROM look-up table. The desired refresh rate, i.e. period, for a particular temperature range is then selected. The control circuit of Hsu thus forms the "clock period controller circuit" that generates a "clock" signal based on the "period control signal" from the ROM look-up table. The ROM look-up table then forms a "calibration circuit" that is responsive to a coding signal. Note that all look-up tables, i.e. registers, require a coding signal. This coding signal determines the period of the refresh clock and thus this coding signal is a "period coding signal". Hsu also as noted above utilizes a temperature sensor that forms part of a "temperature sensor circuit" to sense the temperature of the chip. The temperature sensing circuit of Hsu produces a signal applied to the "clock period controller circuit" (See column 1, around line 60) which causes the "period control signal" from the look-up table to be based on the temperature output signal and the calibration circuit composed of at least the ROM look-up table noted above. Hsu also specifically points out that the temperature sensor "must be calibrated" (See column 2, around line 11). This above structure of Hsu provides for a method for controlling the refresh period of an integrated circuit memory device that controls the refresh clock such that the period control signal is obtained from a look-up table. The above structure of Hsu also provides for changing the period of the clock based upon "variations in the operational temperature of the semiconductor memory device" (See column 1, around line 65).

Hsu while strongly suggesting the use of a calibration circuit for use in the temperature sensing circuit, Hsu does not show the specifics of such a circuit.

Vergis also employs a temperature sensor 102 to sense the temperature of a memory device (See Figure 1 and the abstract of Vergis). Column 2, lines 24-68 and column 3, lines 1-45 of Vergis describes a calibration circuit in the form of a register 104 that provides a calibration constant so that the "temperature signal" from the temperature sensing circuit is accurate. The calibration circuit of Vergis has two states that "first state" (i.e. "test mode") where the sensor is "tested against known parameters" so that the proper data can be written into the calibration circuit 104, via a "coding signal". Also in this "first state" a signal will be produced at the output of the temperature sensor circuit that will be based on a "temperature sensor output control signal", i.e. the known parameter upon which the device is being tested. Normal run conditions define the "second state" in Vergis where the output of the temperature sensor 102 is modified by the calibration circuit 104 to produce a temperature output signal based upon the temperature sensor and the calibration circuit. All registers require a "coding signal" when written with data. This signal is what applicant refers to as a "temperature-coding signal". The output of the "temperature sensor" of either Hsu or Vergis is what applicant calls "an operating temperature signal" or "temperature output signal" or "operational temperature signal". In Vergis the "operating temperature signal" is digital because of the A/D converter 122 and the register 104 thus this signal "comprise a plurality of bits, ones of which correspond to temperature operating ranges of the memory device". The output of the register in Hsu is likewise digital.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide Hsu with a temperature calibration arrangement like that disclosed by Vergis that includes a register 104 so as to adjust the output of the temperature sensor of Hsu to obtain a more accurate measurement of the temperature of the memory device as taught by Vergis.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu and Vergis as applied to claims 1, 12 and 13 above, and further in view of Tillinghast et al. 5,278,796 (Tillinghast).

All the same reasoning as applied against claims 1, 12 and 13 above and the following: Hsu and Vergis are both silent on the refresh clock generator circuit having an oscillator that generates the "refresh clock" with a period based on the period control signal.

Tillinghast discloses a temperature dependent DRAM refresh circuit similar to Hsu. Tillinghast discloses the specific details of the refresh clock generator circuit. Specifically, Tillinghast shows in Figure 1 and describes in the specification a refresh clock composed of an oscillator "OSC" and an encoder "ENCODE" that takes the period control signal and encodes that to a signal the "OSC" can use so the correct refresh rate, i.e. correct period can be selected.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the generic clock circuit of Hsu in combination with Vergis with a clock circuit composed of an oscillator and an encoder so as to generate the "refresh clock" with a period based on the period control signal because, as the reference (Hsu and Vergis) is silent on the specifics of the clock circuit, any art-recognized equivalent refresh clock circuit would have been usable such as the conventional oscillator and encoding unit of Tillinghast.

Claims 2, and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu and Vergis as applied to claims 1, 12 and 13 above, and further in view of Millman "Micro-electronics" (Millman).

All the same reasoning as applied against claims 1, 12 and 13 above and the following: Hsu and Vergis are both silent on the specific make-up of the calibration circuit that makes up in part the temperature sensor circuit. The most detailed description is that it is composed of a register. Hsu and Vergis do not identify the plurality of fuses therein.

Hsu and Vergis also are both silent on the specific make-up of the ROM look-up table that makes up at least in part the calibration circuit of the clock period controller. Hsu and Vergis do not identify a plurality of fuses contained within this ROM look-up table.

A register is a generic term for memory device such as RAM, ROM, etc.. Millman discloses the conventional form for a basic ROM. Namely, a read only device can have "fuses" to represent the data points therein and the coding signal programs the memory device by breaking "cutting" selective fuses as recognized by page 285 of Millman.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the generic memory device that makes up at least in part the calibration circuit of the temperature sensor circuit with a ROM that employs fuses responsive to a coding signal because, as the reference (Hsu and Vergis) is silent on the specifics of the memory device that makes up at least in part the calibration circuit of the temperature sensor circuit, any art recognized memory device would have been usable such as the conventional ROM of Millman that employs fuses responsive to a coding signal.

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have replaced the generic memory device that makes up at least in part the calibration circuit of the clock period controller with a ROM that employs fuses responsive to a coding signal because, as the reference (Hsu and Vergis) is silent on the specifics of the memory device that

makes up at least in part the calibration circuit of the clock period controller, any art-recognized memory device would have been usable such as the conventional ROM of Millman that employs fuses responsive to a coding signal.

As noted above Hsu and Vergis makes obvious an integrated circuit memory device that includes among other things a temperature sensing circuit and a clock period controller. The method steps recited in claims like claim 26 are an obvious consequence of the circuit made obvious above. As noted above the structure made obvious has a temperature sensor circuit that includes a calibration circuit with a plurality of fuses and a clock period controller. The structure made obvious above receives the coding signals for both the calibration circuits. The calibration circuits then will output the correct or "real" temperature and the correct period or rate for the refresh operation respectfully. The step of "generating the refresh clock" wherein the period is controlled in accordance to the operational temperature of the semiconductor, i.e. chip, memory device is clearly provided for as indicated above. The operational temperature signal is digital as indicated above and thus the bits of the signal are enabled and the period controlling signal from the calibration circuit of the clock period controller is generated by receiving the period coding signal, which controls the period of the refresh clock, in response to the enabled operational temperature signal as indicated above. Clearly the coding signal for the calibration circuit of the clock period controller selects the proper refresh rate, or period based upon the temperature sensor circuit's output. As recognized by Hsu selecting the refresh period based upon the temperature allows for the saving of energy. The structure made obvious above outputs a digital sensor output signal, i.e the signal output from the temperature calibration circuit by receiving the sensor coding signal and sensing the real operational temperature from the temperature sensor directly.

Allowable Subject Matter

Claims 4-11, and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant's arguments filed 8-11-2003 have been fully considered but they are not persuasive. Applicant believes that the temperature sensor circuit of Vergis does not

have two states. The examiner respectfully disagrees. See page 3 of the previous office action.

Claims 18-25, 27-32 are allowed.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. Shingleton whose telephone number is 703-308-4903. The examiner can normally be reached on Monday-Thursday from 8:00 to 4:30. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal, can be reached on (703) 308-4909. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

MBS
Oct 18, 2003

MICHAEL B. SINGLETON
PRIMARY EXAMINER
GROUP ART UNIT 2817